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Chua-Chin Wang; Ya-Hsin Hsueh; Yi-Wei Chen;
Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on
Volume 2, 26-29 May 2002 Page(s):II-772 - II-775 vol.2
Digital Object Identifier 10.1109/ISCAS.2002.1011467

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☐   2. **Multilevel magnetoresistive random access memory written at Curie poin**
Zheng, Y.K.; Wu, Y.H.; Qiu, J.J.; Guo, Z.B.; Han, G.C.; Li, K.B.; Lu, Z.Q.; Xie, I
Magnetics Conference, 2002. INTERMAG Europe 2002. Digest of Technical P
International
28 April-2 May 2002 Page(s):BB2
Digital Object Identifier 10.1109/INTMAG.2002.1000778

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☐   3. **Split FIFO phase synchronization for high speed interconnect**
Jex, J.; Nag, P.; Burton, T.; Mooney, R.;
Communications, Computers, and Signal Processing, 1995. Proceedings. IEEI
Conference on
17-19 May 1995 Page(s):66 - 69
Digital Object Identifier 10.1109/PACRIM.1995.519411

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☐	L8	((auxilliary or secondar$3) near3 (fifo or memor$3)) and ((rout$3 or swap$4 or exchang$3) near4 ((write near2 point$3) same (read near3 point$2)))	0
☐	L7	((auxilliary or secondar$3) near3 (fifo or memor$3)) and ((rout$3 or swap$4 or exchang$3) near4 (access near4 point$))	37
☐	L6	((auxilliary or secondar$3) near3 (fifo or memor$3)) same ((rout$3 or swap$4 or exchang$3) near4 (access near4 point$))	2
☐	L5	(auxilliary near3 (fifo or memor$3)) and(access near4 point$3)	4
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